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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,918	09/22/2003	Masanori Ogura	03500.017569.	5148

5514 7590 12/28/2006

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EXAMINER	
KHAN, USMAN A	
ART UNIT	**PAPER NUMBER**
2622	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/28/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/664,918	OGURA ET AL.	
	Examiner	Art Unit	
	Usman Khan	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

The information disclosure statements (IDS) submitted on 12/19/2003, 10/18/2005, and 12/02/2005 have been considered by the examiner. The submissions are in compliance with the provisions of 37 CFR 1.97.

Drawings

Figures 7A, 7B, and 8 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objection

Claims 2, 3, 5, 6, 7, 8 are objected to because of the following informalities: each of these dependent claims should start with "The" since these dependent claims reference back to a solid state image pick-up device of the independent claims from which they depend. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 - 2 and 5 - 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki (US PgPub 2002/0025164) in further view of Applicants admitted prior art.

Regarding **claim 1,** Suzuki teaches a solid state image pick-up device formed on a chip (paragraph 0001 *et seq.*), comprising: a pixel region (figure 1 item 110A); a pad for outputting an output of the amplifier to an outside of the chip (figure 1, items 110B, 115B, and 116B; also paragraph 0060, the shading pixel signals from 110B are sent through the amplifier 115B and output to pad electrode 116B; this pad electrode is located near the right vertical side of the pixel array). an amplifier for amplifying the signal charge read from the pixel region (figure 1, items 110B and 115B; also paragraph 0060, the shading pixel signals from 110B are sent through the amplifier 115B).

However, Suzuki fails to disclose that a first shift register for reading a signal charge from the pixel region, a second shift register; wherein the first and second shift registers are arranged along respectively different side portions of the chip. the amplifier for amplifying the signal charge read from the pixel region by the first shift register. The pad being arranged along a side portion of the chip different from the side portion along which the first shift register is arranged. The second shift register having a lower driving frequency than that of the first shift register. Applicants admitted prior art, on the other hand teaches that a first shift register for reading a signal charge from the pixel region, a second shift register; wherein the first and second shift registers are arranged along respectively different side portions of the chip. the amplifier for amplifying the signal charge read from the pixel region by the first shift register. The pad being arranged along a side portion of the chip different from the side portion along which the first shift register is arranged. The second shift register having a lower driving frequency than that of the first shift register.

More specifically, admitted prior art teaches a first shift register for reading a signal charge from the pixel region (figure 8, item 205), a second shift register (figure 8, item 202); wherein the first and second shift registers are arranged along respectively different side portions of the chip (figure 8). the amplifier for amplifying the signal charge read from the pixel region by the first shift register (figure 8 item 207). The pad being arranged along a side portion of the chip different from the side portion along which the first shift register is arranged (when applicants admitted prior art is combined with Suzuki invention the pad of Suzuki will be arranged along a side portion of the chip

different from the side portion along which the horizontal (i.e. first) shift register is located. The second shift register having a lower driving frequency than that of the first shift register (paragraph 0014).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to applicants admitted prior art of horizontal and vertical shift registers with the teachings of Suzuki to have a simple and reliable way of addressing and reading out pixels.

Regarding **claim 2**, as mentioned above in the discussion of claim 1, Suzuki in further view of applicant admitted prior art teaches all of the limitations of the parent claim. Additionally, Suzuki teaches that the pixel region, pixels having an active element are two-dimensionally arranged (figure 1 item 110A).

Regarding **claim 5**, as mentioned above in the discussion of claim 2, Suzuki in further view of applicant admitted prior art teaches all of the limitations of the parent claim. Additionally, Suzuki teaches that the pixel region is formed into a rectangle, and the first shift register is arranged closer to a long side of the pixel region (figure 1).

Regarding **claim 6**, as mentioned above in the discussion of claim 5, Suzuki in further view of applicant admitted prior art teaches all of the limitations of the parent claim. Additionally, applicant admitted prior art teaches that the pixel region is

sandwiched by shift registers (figure 8, shift register 202 and 205 in essence sandwich the region close to where they form a right angle to each other).

Regarding **claim 7**, as mentioned above in the discussion of claim 2, Suzuki in further view of applicant admitted prior art teaches all of the limitations of the parent claim. Additionally, applicant admitted prior art teaches that the first shift register is a horizontal shift register (figure 8, item 205), and the second shift register is a vertical shift register (figure 8, item 202).

Regarding **claim 8**, Suzuki teaches a camera with a solid state image pick-up device formed on a chip (paragraph 0001 *et seq.*), comprising: a pixel region (figure 1 item 110A); a pad for outputting an output of the amplifier to an outside of the chip (figure 1, items 110B, 115B, and 116B; also paragraph 0060, the shading pixel signals from 110B are sent through the amplifier 115B and output to pad electrode 116B; this pad electrode is located near the right vertical side of the pixel array). An amplifier for amplifying the signal charge read from the pixel region (figure 1, items 110B and 115B; also paragraph 0060, the shading pixel signals from 110B are sent through the amplifier 115B). A lens for forming an optical image of a subject (figure, 19); and a signal-processing unit for processing a signal from the solid-state image pick-up device (figure 16, item 221 controlling the processing of the various components in the camera which in turn controls the processing of the signals).

However, Suzuki fails to disclose that a first shift register for reading a signal charge from the pixel region, a second shift register; wherein the first and second shift registers are arranged along respectively different side portions of the chip. The amplifier for amplifying the signal charge read from the pixel region by the first shift register. The pad being arranged along a side portion of the chip different from the side portion along which the first shift register is arranged. The second shift register having a lower driving frequency than that of the first shift register. Applicants admitted prior art, on the other hand teaches that a first shift register for reading a signal charge from the pixel region, a second shift register; wherein the first and second shift registers are arranged along respectively different side portions of the chip. The amplifier for amplifying the signal charge read from the pixel region by the first shift register. The pad being arranged along a side portion of the chip different from the side portion along which the first shift register is arranged. The second shift register having a lower driving frequency than that of the first shift register.

More specifically, admitted prior art teaches a first shift register for reading a signal charge from the pixel region (figure 8, item 205), a second shift register (figure 8, item 202); wherein the first and second shift registers are arranged along respectively different side portions of the chip (figure 8). the amplifier for amplifying the signal charge read from the pixel region by the first shift register (figure 8 item 207). The pad being arranged along a side portion of the chip different from the side portion along which the first shift register is arranged (when applicants admitted prior art is combined with Suzuki invention the pad of Suzuki will be arranged along a side portion of the chip

different from the side portion along which the horizontal (i.e. first) shift register is located. The second shift register having a lower driving frequency than that of the first shift register (paragraph 0014).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to applicants admitted prior art of horizontal and vertical shift registers with the teachings of Suzuki to have a simple and reliable way of addressing and reading out pixels.

Regarding **claim 9,** Suzuki teaches a solid-state image pick-up device formed on a chip (paragraph 0001 *et seq.*), comprising: a pixel region (figure 1 item 110A); a pad for supplying a voltage to the amplifier (figure 1, items 110B, 115B, and 116B; also paragraph 0060 *et seq.*; this pad electrode is located near the right vertical side of the pixel array). An amplifier for amplifying the signal charge read from the pixel region (figure 1, items 110B and 115B; also paragraph 0060, the shading pixel signals from 110B are sent through the amplifier 115B).

However, Suzuki fails to disclose that a first shift register for reading a signal charge from the pixel region, a second shift register; wherein the first and second shift registers are arranged along respectively different side portions of the chip. The amplifier for amplifying the signal charge read from the pixel region by the first shift register. The pad being arranged along a side portion of the chip different from the side portion along which the first shift register is arranged. The second shift register having a lower driving frequency than that of the first shift register. Applicants admitted prior

art, on the other hand teaches that a first shift register for reading a signal charge from the pixel region, a second shift register; wherein the first and second shift registers are arranged along respectively different side portions of the chip. The amplifier for amplifying the signal charge read from the pixel region by the first shift register. The pad being arranged along a side portion of the chip different from the side portion along which the first shift register is arranged. The second shift register having a lower driving frequency than that of the first shift register.

More specifically, admitted prior art teaches a first shift register for reading a signal charge from the pixel region (figure 8, item 205), a second shift register (figure 8, item 202); wherein the first and second shift registers are arranged along respectively different side portions of the chip (figure 8). the amplifier for amplifying the signal charge read from the pixel region by the first shift register (figure 8 item 207). The pad being arranged along a side portion of the chip different from the side portion along which the first shift register is arranged (when applicants admitted prior art is combined with Suzuki invention the pad of Suzuki will be arranged along a side portion of the chip different from the side portion along which the horizontal (i.e. first) shift register is located. The second shift register having a lower driving frequency than that of the first shift register (paragraph 0014).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to applicants admitted prior art of horizontal and vertical shift registers with the teachings of Suzuki to have a simple and reliable way of addressing and reading out pixels.

Regarding **claim 10,** Suzuki teaches a solid-state image pick-up device formed on a chip (paragraph 0001 *et seq.*), comprising: a pixel region (figure 1 item 110A); a pad for supplying a predetermined voltage or a ground voltage to an active element included in a pixel in the pixel region (figure 1, items 110B, 115B, and 116B; also paragraph 0060 *et seq.*; this pad electrode is located near the right vertical side of the pixel array). An amplifier for amplifying the signal charge read from the pixel region (figure 1, items 110B and 115B; also paragraph 0060, the shading pixel signals from 110B are sent through the amplifier 115B).

However, Suzuki fails to disclose that a first shift register for reading a signal charge from the pixel region, a second shift register; wherein the first and second shift registers are arranged along respectively different side portions of the chip. The amplifier for amplifying the signal charge read from the pixel region by the first shift register. The pad being arranged along a side portion of the chip different from the side portion along which the first shift register is arranged. The second shift register having a lower driving frequency than that of the first shift register. Applicants admitted prior art, on the other hand teaches that a first shift register for reading a signal charge from the pixel region, a second shift register; wherein the first and second shift registers are arranged along respectively different side portions of the chip. The amplifier for amplifying the signal charge read from the pixel region by the first shift register. The pad being arranged along a side portion of the chip different from the side portion along

which the first shift register is arranged. The second shift register having a lower driving frequency than that of the first shift register.

More specifically, admitted prior art teaches a first shift register for reading a signal charge from the pixel region (figure 8, item 205), a second shift register (figure 8, item 202); wherein the first and second shift registers are arranged along respectively different side portions of the chip (figure 8). the amplifier for amplifying the signal charge read from the pixel region by the first shift register (figure 8 item 207). The pad being arranged along a side portion of the chip different from the side portion along which the first shift register is arranged (when applicants admitted prior art is combined with Suzuki invention the pad of Suzuki will be arranged along a side portion of the chip different from the side portion along which the horizontal (i.e. first) shift register is located. The second shift register having a lower driving frequency than that of the first shift register (paragraph 0014).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to applicants admitted prior art of horizontal and vertical shift registers with the teachings of Suzuki to have a simple and reliable way of addressing and reading out pixels.

Claims 3 and 11 - 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki (US PgPub 2002/0025164) in further view of applicants admitted prior art in further view of Itano et al. (US PgPub 2002/0051071).

Regarding **claim 3**, as mentioned above in the discussion of claim 2, Suzuki in further view of applicant admitted prior art teaches all of the limitations of the parent claim. However, Suzuki in further view of applicant admitted prior art fail to disclose that the active element comprises at least one selected from the group consisting of a transfer MOS transistor, a reset MOS transistor, a source follower input MOS transistor, and a selection MOS transistor. Itano et al., on the other hand teaches that the active element comprises at least one selected from the group consisting of a transfer MOS transistor, a reset MOS transistor, a source follower input MOS transistor, and a selection MOS transistor.

More specifically, Itano et al. teaches the active element comprises at least one selected from the group consisting of a transfer MOS transistor (figure 1 item 105, and paragraph 0006), a reset MOS transistor (figure 1 items 110a and 110b, and paragraph 0006), a source follower input MOS transistor (figure 1 item 107, and paragraphs 0006, 0048, 0051), and a selection MOS transistor (paragraph 0051).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Itano et al. with the teachings of Suzuki in further view of applicant admitted prior art for reduction of size and in turn cost as taught in paragraph 0021 of Itano et al.

Regarding **claims 11 - 13**, as mentioned above in the discussion of claims 1, 9, and 10 respectively, Suzuki in further view of applicant admitted prior art teaches all of the limitations of the parent claims. Additionally, Itano et al. teaches that the side

portions along which the first and second shift registers are arranged are adjacent to each other (figure 1, 108, 109a, and 109b).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Itano et al. with the teachings of Suzuki in further view of applicant admitted prior art for reduction of size and in turn cost as taught in paragraph 0021 of Itano et al.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ichikawa et al. (US patent No. 6,559,821) pads are arranged near the vertical shift register of a LCD display.

Watanabe et al. (US patent No. 6,476,897) pads are arranged near the vertical shift register of a LCD display.

Usami et al. (US patent No. 5,391,501) pads are arranged all around an image pickup element.

Hiyama et al. (US PgPub 2002/0024001) pads are arranged all around an image pickup element.

Ichikawa et al. (US PgPub 2002/0036606) pads are arranged near the vertical shift register of a LCD display.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Usman Khan whose telephone number is (571) 270-1131. The examiner can normally be reached on Mon-Thru 6:45-4:15; Fri 6:45-3:15 or Alt. Fri off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Usman Khan
12/08/2006
Patent Examiner
Art Unit 2622

DAVID OMETZ
SUPERVISORY PATENT EXAMINER